CLAIMS

What is claimed is:

1. A hybrid microelectronic array structure comprising:

a microelectronic integrated circuit array comprising an array of microelectronic integrated circuits, each of the microelectronic integrated circuits comprising a first supported-structure interconnect location and a second supported-structure interconnect location;

a supported array comprising an array of supported islands with each supported island having at least one supported element therein, there being at least one supported element for each of the microelectronic integrated circuits, each of the supported elements comprising a first region and a second region, wherein

the first region of each of the supported islands is physically discontinuous from the first region of each of the other supported islands, and

the second region of each of the supported islands is physically discontinuous from the second region of each of the other supported islands; and

a bump interconnect structure extending between each of the microelectronic integrated circuits and its respective supported element, each bump interconnect structure comprising

a first bump interconnect extending from the first supported-structure interconnect location of each of the microelectronic integrated circuits to the first region of its respective supported element, and

a second bump interconnect extending from the second supported-structure interconnect location of each of the microelectronic integrated circuits to the second region of its respective supported element.

2. The hybrid microelectronic array structure of claim 1, wherein the first region comprises a first semiconductor region and the second region comprises a second semiconductor region.

3. The hybrid microelectronic array structure of claim 1, wherein each

microelectronic integrated circuit comprises

an electrical interface circuit, and

wherein each supported element comprises

an input/output element supported on the electrical interface circuit.

4. The hybrid microelectronic array structure of claim 3, wherein the electrical interface circuit is a readout integrated circuit, and the input/output element is a detector.

5. The hybrid microelectronic array structure of claim 3, wherein the electrical interface circuit is a driver integrated circuit, and the input/output element is an emitter.

6. The hybrid microelectronic array structure of claim 1, wherein the hybrid microelectronic array structure is planar.

7. The hybrid microelectronic array structure of claim 1, wherein the hybrid microelectronic array structure is curved.

8. A hybrid microelectronic array structure comprising:

a readout integrated circuit array comprising an array of readout integrated circuits, each of the readout integrated circuits comprising a first detector interconnect location and a second detector interconnect location;

a detector array comprising an array of detector islands with each detector island having at least one detector element therein, there being at least one respective detector element for each of the readout integrated circuits, each of the detector elements comprising a first semiconductor region and a second semiconductor region, wherein

the first semiconductor region of each of the detector islands is physically discontinuous from the first semiconductor region of each of the other detector islands, and

the second semiconductor region of each of the detector islands is

physically discontinuous from the second semiconductor region of each of the other detector islands; and

a bump interconnect structure extending between each of the readout integrated circuits and its respective detector element, each bump interconnect structure comprising

a first bump interconnect extending from the first detector interconnect location of each of the readout integrated circuits to the first semiconductor region of its respective detector element, and

a second bump interconnect extending from the second detector interconnect location of each of the readout integrated circuits to the second semiconductor region of its respective detector element.

9. The hybrid microelectronic array structure of claim 8, wherein

the first semiconductor region of each of the detector islands is an n-doped semiconductor, and

the second semiconductor region of each of the detector islands is a p-doped semiconductor.

10. The hybrid microelectronic array structure of claim 8, wherein the hybrid microelectronic array structure further comprises

an electrically nonconducting support material lying between the readout integrated circuit array and the detector array.

11. The hybrid microelectronic array structure of claim 8, wherein the readout integrated circuit array comprises

an electrical conductor interconnecting all of the first detector interconnect locations.

12. The hybrid microelectronic array structure of claim 8, wherein the readout integrated circuit array and the detector array are each substantially planar.

13. The hybrid microelectronic array structure of claim 8, wherein the readout integrated circuit array and the detector array are each curved.

14. The hybrid microelectronic array structure of claim 8, wherein the first bump interconnect and the second bump interconnect each comprise the element indium.

15. The hybrid microelectronic array structure of claim 8, wherein the detector array type is selected is selected from the group consisting of mercury-cadmium-telluride, indium antimonide, quantum well infrared photodetector, and extrinsic impurity band conductor material.

16. A hybrid microelectronic array structure comprising:

a readout integrated circuit array comprising an array of readout integrated circuits, each of the readout integrated circuits comprising a first detector interconnect location and a second detector interconnect location;

a detector array comprising an array of detector islands with each detector island having at least one detector element therein, there being at least one respective detector element for each of the readout integrated circuits, each of the detector elements comprising a first semiconductor region and a second semiconductor region, and wherein each of the detector islands is electrically isolated from each of the other detector islands except through the readout integrated circuit array; and

an interconnect structure extending between each of the readout integrated circuits and its respective detector element, each interconnect structure comprising

a first interconnect extending from the first detector interconnect location of each of the readout integrated circuits to the first semiconductor region of its respective detector element, and

a second interconnect extending from the second detector interconnect location of each of the readout integrated circuits to the second semiconductor region of its respective detector element.

17. The hybrid microelectronic array structure of claim 16, wherein the first interconnect and the second interconnect of each interconnect structure are each electrically conducting bump interconnects.

18. A method of fabricating a hybrid microelectronic array structure, comprising the steps of

providing a readout integrated circuit array comprising an array of readout integrated circuits, each of the readout integrated circuits comprising a first detector interconnect location and a second detector interconnect location;

preparing a detector array comprising an array of detector islands with each detector island having at least one detector element therein, there being a respective detector element for each of the readout integrated circuits, each of the detector islands comprising a first semiconductor region and a second semiconductor region, the step of providing a detector array including the steps of

depositing the first semiconductor region onto a detector substrate and depositing the second semiconductor region onto the first semiconductor region,

defining detector islands as electrically isolated segments, each detector island including a segment of the first semiconductor region overlying the detector substrate, and the second semiconductor region overlying the first semiconductor region,

forming on each detector element a first interconnect to the first semiconductor region and a second interconnect to the second semiconductor region; and

joining the detector array to the readout integrated circuit array by an interconnect structure to form the hybrid microelectronic array structure, with each readout integrated electrically interconnected to the respective one of the detector elements, the step of joining including the steps of

joining each first interconnect to the respective first detector interconnect location, and

joining each second interconnect to the respective second detector

interconnect location.

19. The method of claim 18, wherein the first interconnect and the second interconnect of each interconnect structure are each electrically conducting bump interconnects.

20. The method of claim 18, wherein the step of defining detector islands includes the step of

forming a trench through the first semiconductor region and through the semiconductor region and into the detector substrate.

21. The method of claim 18, including an additional step, after the step of preparing and before the step of joining, of

removing the detector substrate.

22. The method of claim 18, including an additional step, after the step of joining, of

deforming the hybrid microelectronic array structure into a curved geometry.

23. The method of claim 18, wherein the readout integrated circuit array comprises

an electrical conductor interconnecting all of the first detector interconnect locations.